Aryabhatta Knowledge University (AKU)

Electrical Engineering

Analog Electronic Circuits

Solved Exam Paper 2019

Question. State the Barkhausen condition for an electronic system to oscillate with feedback

Answer: Conditions which are required to be satisfied to operate the circuit as an oscillator are called as “Barkhausen criterion” for sustained oscillations.

The Barkhausen criteria should be satisfied by an amplifier with positive feedback to ensure the sustained oscillations.

For an oscillation circuit, there is no input signal “Vs”, hence the feedback signal Vf itself should be sufficient to maintain the oscillations.

The Barkhausen criterion states that:

• The loop gain is equal to unity in absolute magnitude, that is, $| \beta A | = 1$ and

• The phase shift around the loop is zero or an integer multiple of 2π: $\angle \beta A = 2 \pi n, n \in 0, 1, 2,....$

The product β A is called as the “loop gain”.

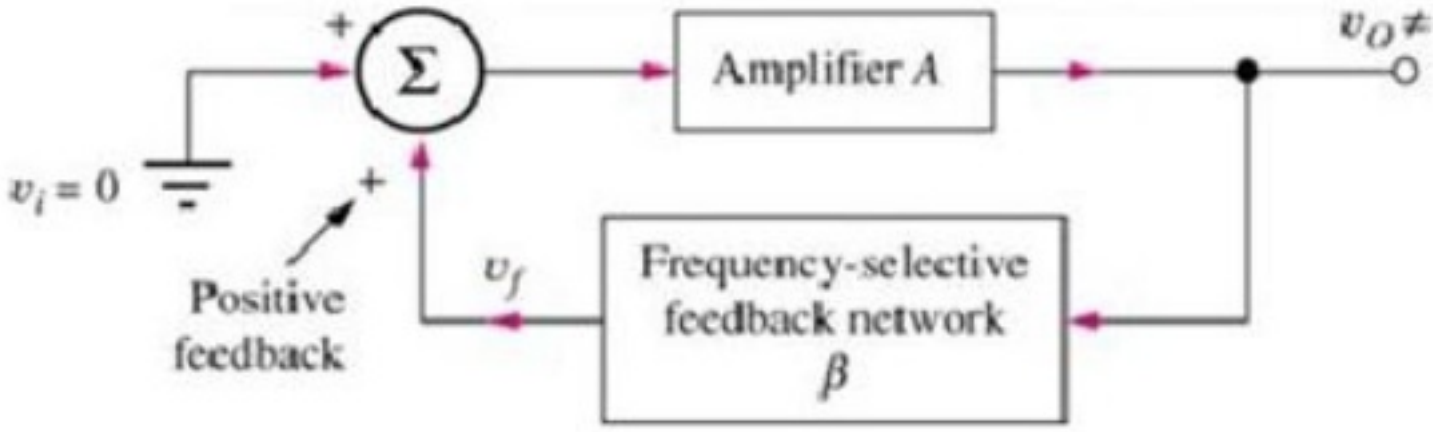


Fig1: Barkhausen's criteria for oscillations

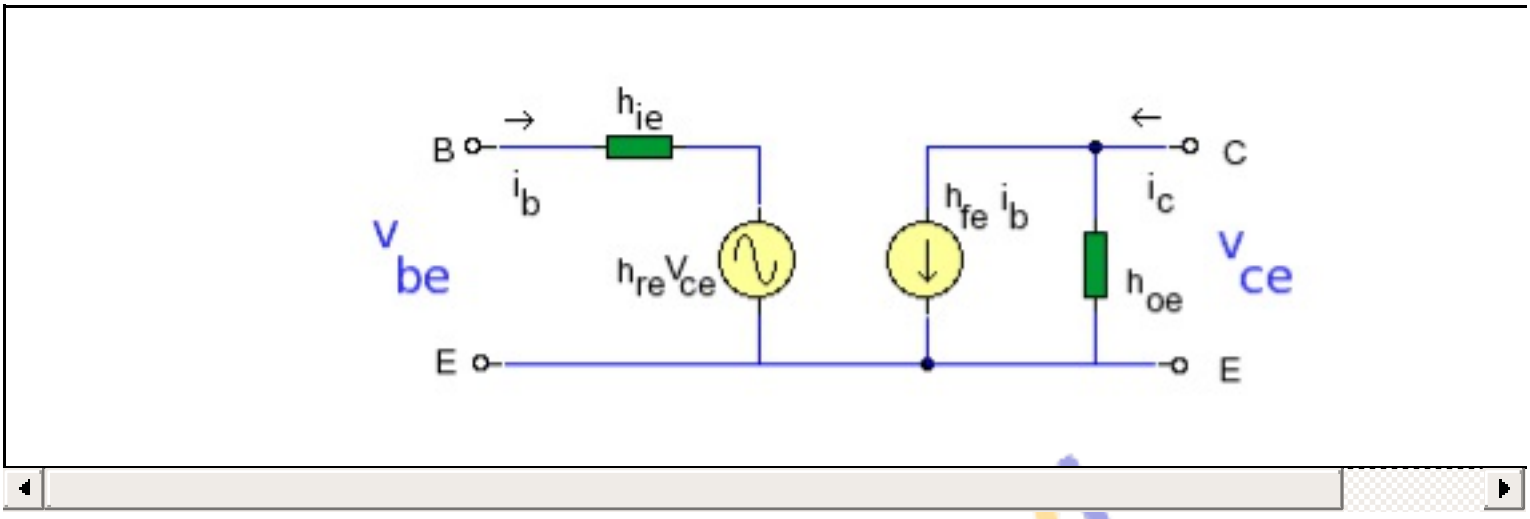
Question. Derive an expression for input impedance, output impedance, voltage gain and current gain of the transistor amplifier using h-parameters

Answer: The hybrid model has four h-parameters. The "h" stands for hybrid because the parameters are a mix of impedance, admittance and dimensionless units. In common emitter the parameters are:

h_{ie}	input impedance (Ω)
h_{re}	reverse voltage ratio (dimensionless)
h_{fe}	forward current transfer ratio (dimensionless)
h_{oe}	output admittance (Siemen)

Note that lower case suffixes indicate small signal values and the last

suffix indicates the mode so h_{ie} is input impedance in common emitter, h_{fb} would be forward current transfer ration in common base mode, etc. The hybrid model for the BJT in common emitter mode is shown below:



The hybrid model is suitable for small signals at mid band and describes the action of the transistor. Two equations can be derived from the diagram, one for input voltage v_{be} and one for the output i_c:

$$v_{be} = h_{ie}\ i_b + h_{re}\ v_{ce}$$
$$i_c = h_{fe}\ i_b + h_{oe}\ v_{ce}$$

If i_b is held constant (ib=0) then h_{re} and h_{oe} can be solved:

$$h_{re} = v_{be} / v_{ce} \mid i_b = 0$$
$$h_{oe} = i_c / v_{ce} \mid i_b = 0$$

Also if v_{ce} is held constant (v_{ce}=0) then h_{ie} and h_{fe} can be solved:

$$h_{ie} = v_{be} / i_b \mid v_{ce} = 0$$
$$h_{fe} = i_c / i_b \mid v_{ce} = 0$$

These are the four basic parameters for a BJT in common emitter. Typical values are h_{re} = 1 x10^{-4}, h_{oe} typical value 20uS, h_{ie} typically 1k

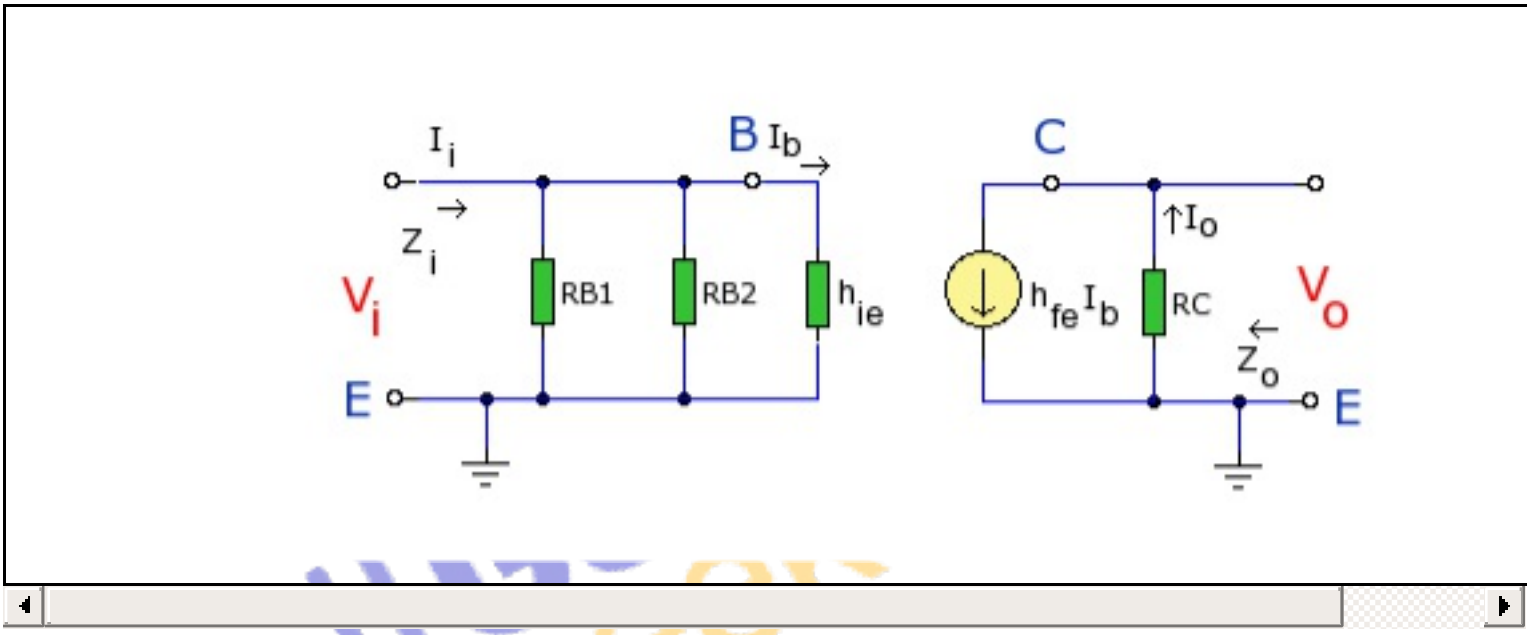
to 20k and h_{fe} can be 50 - 750. The H-parameters can often be found on the transistor datasheets. The table below lists the four h-parameters for the BJT in common base and common collector (emitter follower) mode.

Common Base	Common Emitter	Common Collector	Definitions
$h_{ib} = \frac{v_{eb}}{i_e}$	$h_{ie} = \frac{v_{be}}{i_b}$	$h_{ic} = \frac{v_{bc}}{i_b}$	Input Impedance with Output Short Circuit
$h_{rb} = \frac{v_{eb}}{v_{cb}}$	$h_{re} = \frac{v_{be}}{v_{ce}}$	$h_{rc} = \frac{v_{bc}}{v_{ec}}$	Reverse Voltage Ratio Input Open Circuit
$h_{fb} = \frac{i_c}{i_e}$	$h_{fe} = \frac{i_c}{i_b}$	$h_{fc} = \frac{i_e}{i_b}$	Forward Current Gain Output Short Circuit
$h_{ob} = \frac{i_c}{v_{cb}}$	$h_{oe} = \frac{i_c}{v_{ce}}$	$h_{oc} = \frac{i_e}{v_{ec}}$	Output Admittance Input Open Circuit

H-parameters are not constant and vary with temperature, collector

current and collector emitter voltage. For this reason when designing a circuit the hybrid parameters should be measured under the same conditions as the actual circuit.

The small signal parameter $h_{re}V_{ce}$ is often too small to be considered so the input resistance is just h_{ie}. Often the output resistance h_{oe} is often large compared wi the the collector resistor RC and its effects can be ignored. The h-parameter equivalent model is now simplified and drawn below:



Input Impedance Z_i

The input impedance is the parallel combination of bias resistors RE RB2. As the power supply is considered short circuit at small signal then RB1 and RB2 are in parallel. RBB will represent the p combination:

$$R_{BB} = RB1 \,||\, RB2 = \frac{RB1}{RB1 +}$$

	RB2

As R_{BB} is in parallel with h_{ie} then:

$Z_i = R_{BB} \parallel h_{ie}$

Output Impedance Z_o

As $h_{fe}I_b$ is an ideal current generator with infinite output impedance output impedance looking into the circuit is:

$Z_o = RC$

Voltage Gain A_v

Note the − sign in the equation, this indicates phase inversion of the waveform.

$V_o = -I_o\ RC = -h_{fe}\ I_b\ RC$

as $I_b = V_i / h_{ie}$ then:

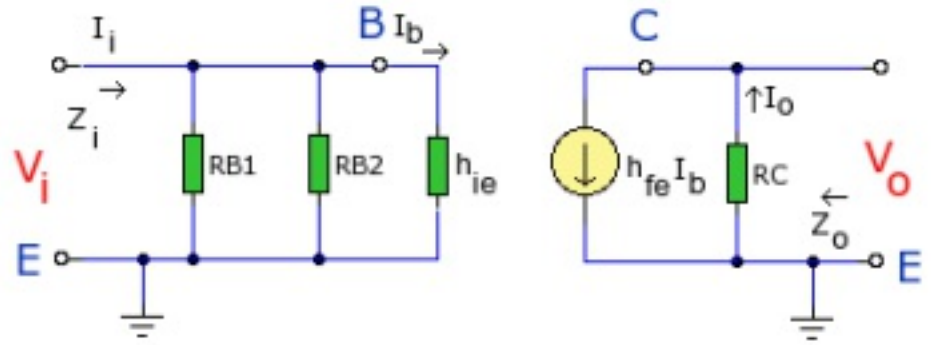
$$= -\frac{V_i}{h_{fe}}\ RC$$

$$= \frac{-h_{fe}\ RC}{h_{ie}}\ V_i$$

$$A_v = \frac{V_o}{V_i} = \frac{-h_{fe}\ RC}{h_{ie}}$$

Current Gain A_i

The current gain is the ratio Io / Ii. At the input the current is split be the parallel branch R_{BB} and h_{ie}. So looking at the equivalent h-para model again (shown below):



The current divider rule can be used for I_b:

$$I_b = \frac{R_{BB}\, I_i}{R_{BB} + h_{ie}}$$

$$\frac{I_b}{I_i} = \frac{R_{BB}}{R_{BB} + h_{ie}}$$

At the output side, $I_o = h_{fe}\, I_b$

re-arranging $I_o / I_b = h_{fe}$

$$A_i = \frac{I_o}{I_i} = \frac{I_o\ I_b}{I_b\ I_i} = h_{fe}\ \frac{R_{BB}}{R_{BB} + h_{ie}}$$

$$A_i = \frac{R_{BB}\ h_{fe}}{R_{BB} + h_{ie}}$$

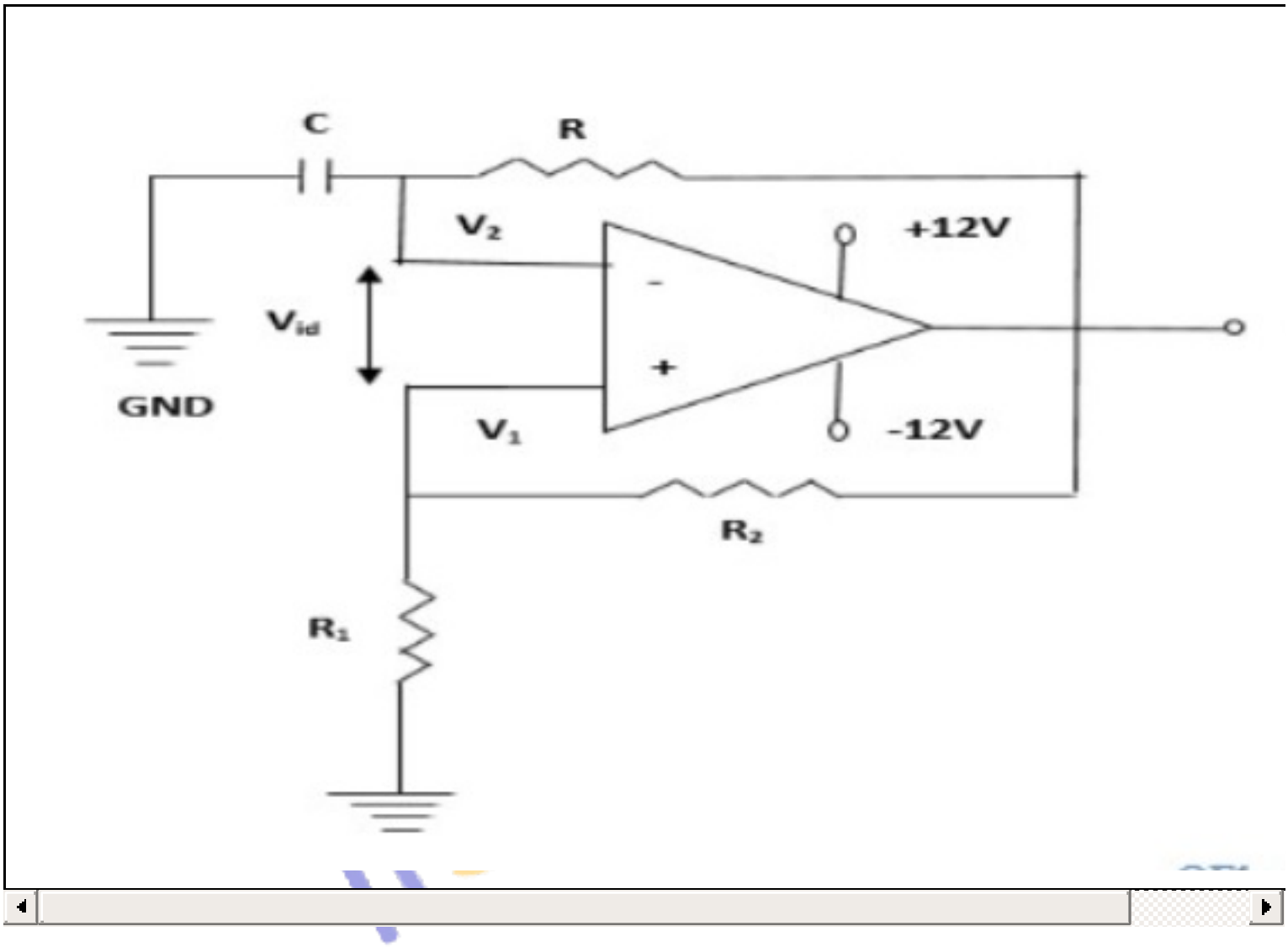
If RBB >> hie then,

$$A_i \approx \frac{R_{BB}\ h_{fe}}{R_{BB}} = h_{fe}$$

Question. With a neat circuit diagram, generate square wave form.

Answer: To design the square wave generator, we need a capacitor, resistor, operational amplifier, and power supply. The capacitor and resistor are connected to the inverting terminal of the operational

amplifier and the resistors R1 and R2 are connected to the non-inverting terminal of the operational amplifier. The circuit diagram of the square wave generator using an operational amplifier is shown below



If we force output to switch between the positive saturation voltage and the negative saturation voltage at the output of an operational amplifier we can achieve square wave as an output wave. Ideally without any input applied the output should be zero, it is expressed as

Vout (output voltage) = 0 V when Vin (input voltage) = 0 V

But practically we get some non-zero output that is expressed as

The Resistors R1 and R2 form a voltage divider network. If the initial output voltage is non-zero we get voltage across Vb. Thus we get a

positive input at the non-inverting terminal and the inverting terminal, then the output gets amplified by its gain and reaches the maximum output voltage thus we get the half of the square wave as shown in figure (a).

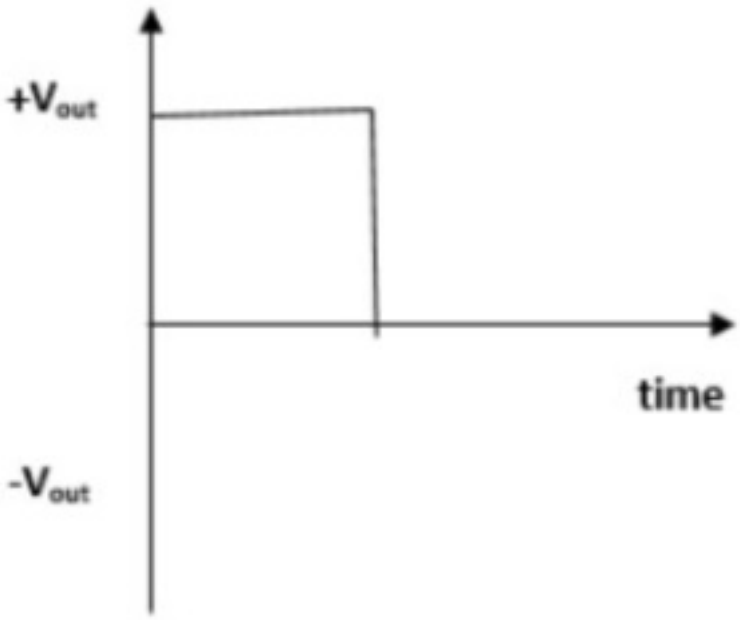


Figure (a)

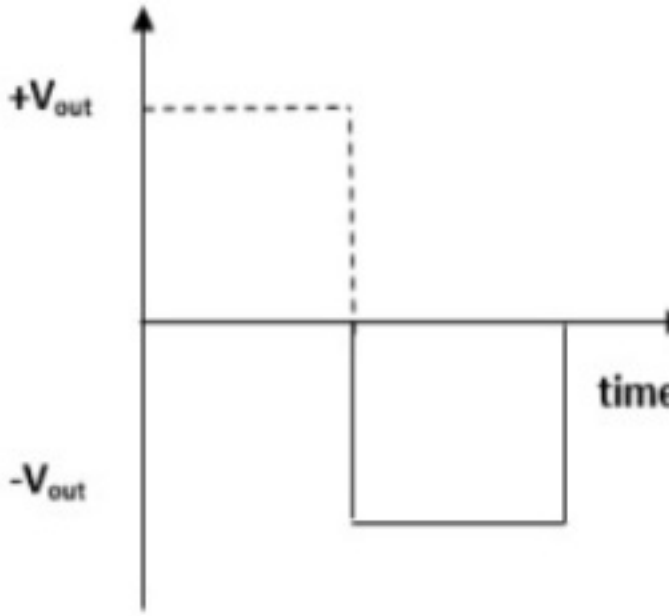
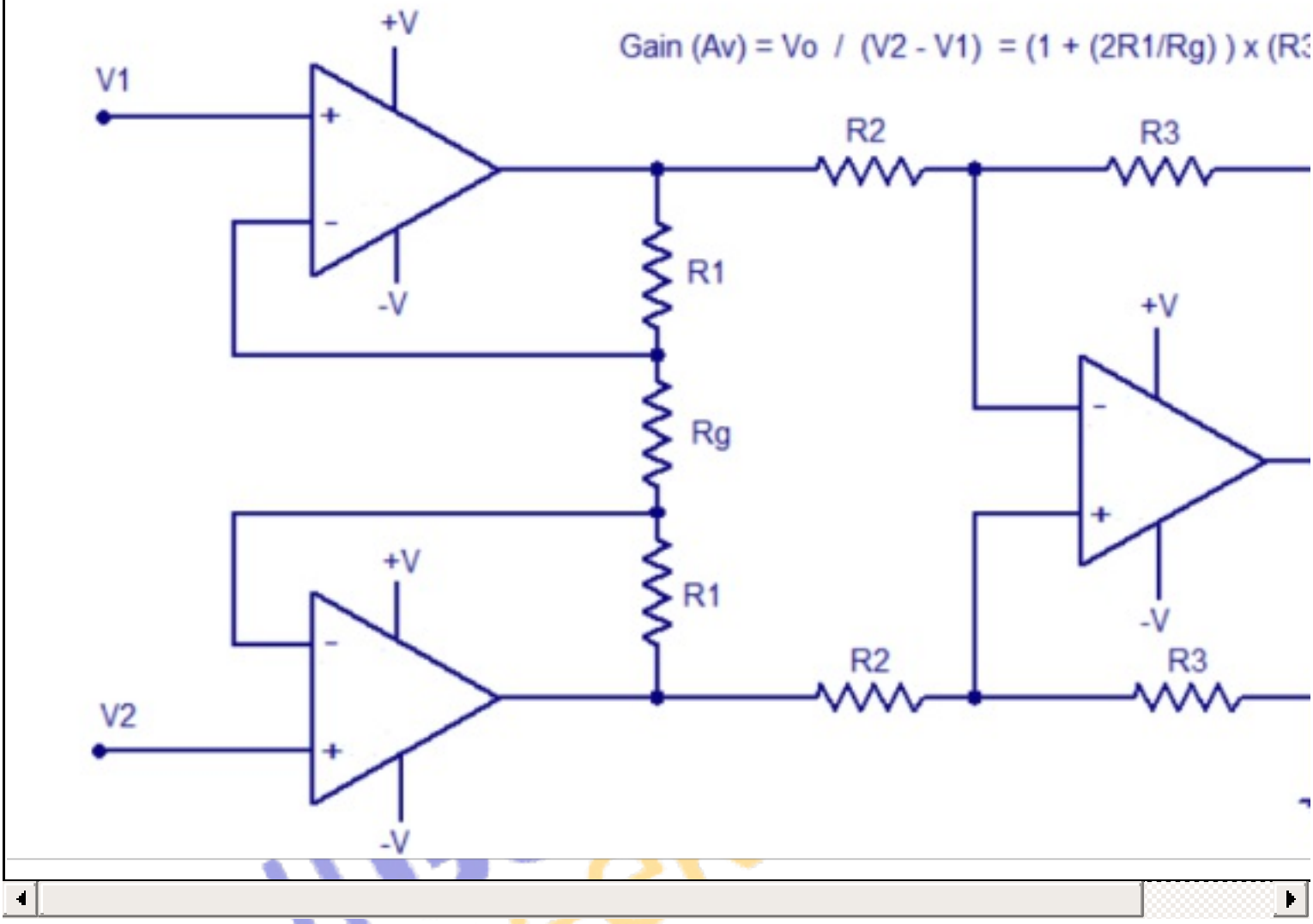


Figure (b)

The capacitor starts charging when we have a non-zero input at the inverting terminal. It will charge continuously until its voltage becomes greater than Vb. As soon as Vc is greater than the Vb (Vc> Vb). The inverting input becomes greater than the non-inverting input and hence op-amp output switches to negative voltage and gets amplified till (–Vout) max. Thus will get the negative half of the square wave as shown in figure (b). This is the application of an op-amp as a square wave generator.

Question. Draw circuit diagram of instrumentation amplifier and obtain an expression of voltage gain

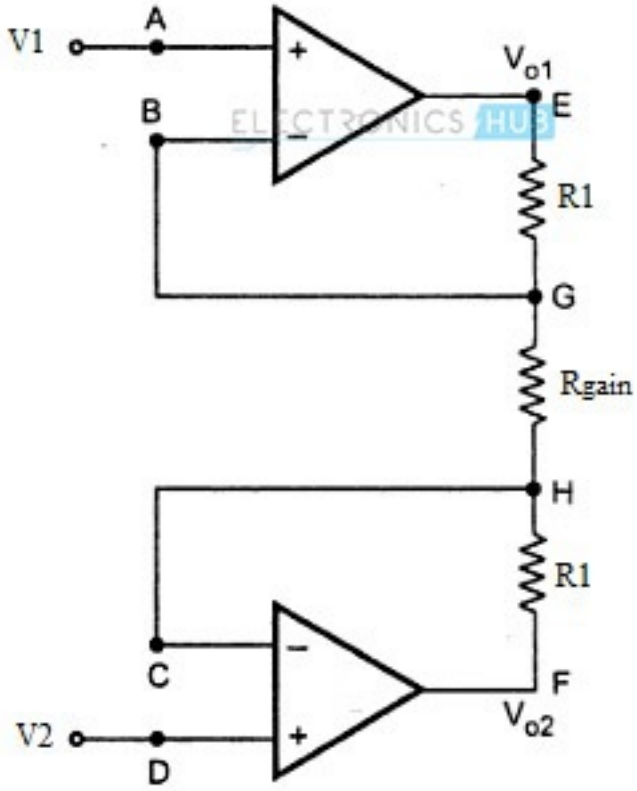
Answer:



The output stage of the instrumentation amplifier is a difference amplifier, whose output Vout is the amplified difference of the input signals applied to its input terminals. If the outputs of op-amp 1 and op-amp 2 are Vo1 and Vo2 respectively, then the output of the difference amplifier is given by,

Vout = (R3/R2)(Vo1-Vo2)

The expressions for Vo1 and Vo2 can be found in terms of the input voltages and resistances. Consider the input stage of the instrumentation amplifier as shown in the figure below.



Input Stage of Instrumentation Amplifier

The potential at node A is the input voltage V1. Hence the potential at node B is also V1, from the virtual short concept. Thus, the potential at node G is also V1.

The potential at node D is the input voltage V2. Hence the potential at node C is also V2, from the virtual short. Thus, the potential at node H is also V2.

Ideally the current to the input stage op-amps is zero. Therefore the current *I* through the resistors R1, Rgain and R1 remains the same.

Applying Ohm's law between the nodes E and F,

$I = (Vo1-Vo2)/(R1+Rgain+R1)$ ———————— 1

$I = (Vo1-Vo2)/(2R1+Rgain)$

Since no current is flowing to the input of the op-amps 1 & 2, the current I between the nodes G and H can be given as,

I = (VG-VH)/Rgain = (V1-V2)/Rgain ——————————- 2

Equating equations 1 and 2,

(Vo1-Vo2)/(2R1+Rgain) = (V1-V2)/Rgain

(Vo1-Vo2) = (2R1+Rgain)(V1-V2)/Rgain ——————— 3

The output of the difference amplifier is given as,

Vout = (R3/R2) (Vo1-Vo2)

Therefore, (Vo1 – Vo2) = (R2/R3)Vout

Substituting (Vo1 – Vo2) value in the equation 3, we get

(R2/R3)Vout = (2R1+Rgain)(V1-V2)/Rgain

i.e. Vout = (R3/R2){(2R1+Rgain)/Rgain}(V1-V2)

The above equation gives the output voltage of an instrumentation amplifier. The overall gain of the amplifier is given by the term (R3/R2){(2R1+Rgain)/Rgain}.

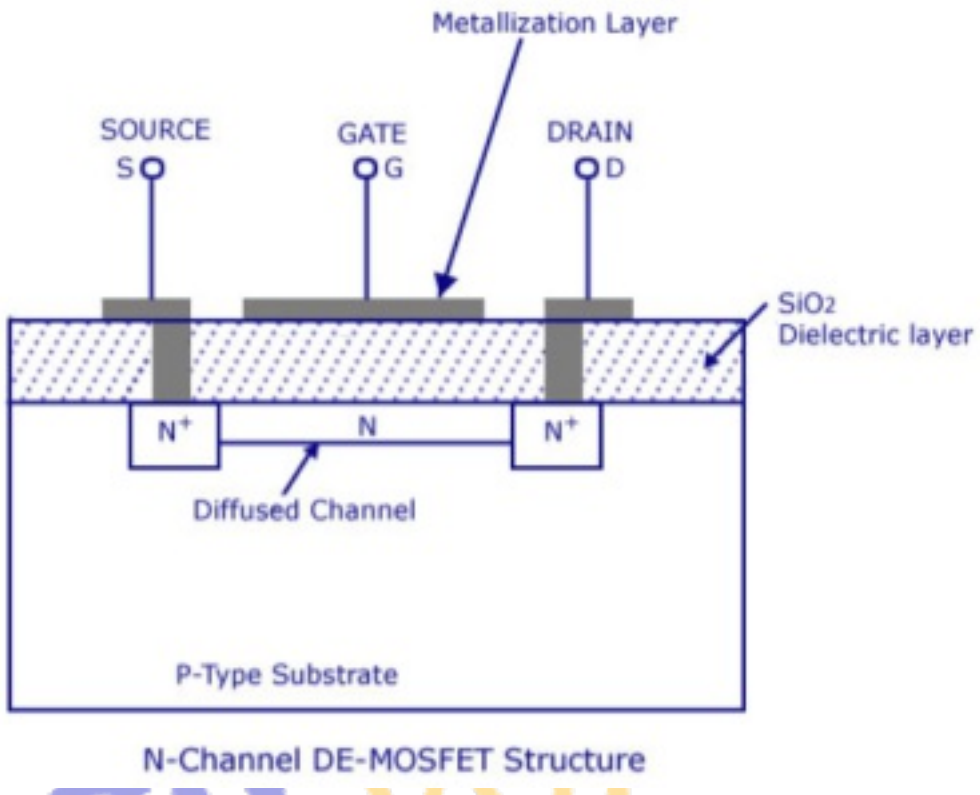
Note:

- The overall voltage gain of an instrumentation amplifier can be controlled by adjusting the value of resistor Rgain.
- The common mode signal attenuation for the instrumentation amplifier is provided by the difference amplifier.

Question. With a neat diagram, explain the construction and operation of depletion MOSFET. Also write the drain and transfer characteristics.

- **Answer:** The basic construction of n-channel depletion type MOSFET is provided in the figure shown above. A slab of p-type material is formed from a silicon base and is referred to as the

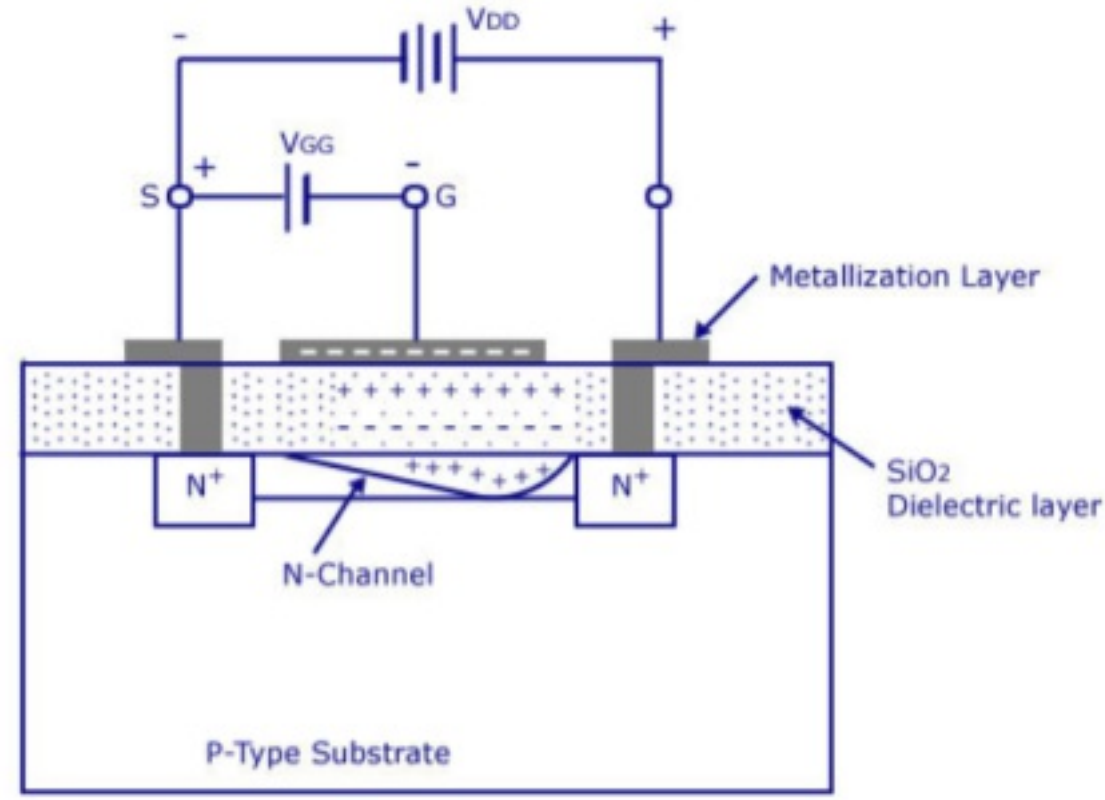
substrate.



N-Channel DE-MOSFET Structure

- It is the foundation upon which the device will be constructed.In some cases the substrate is internally connected to the source terminal. However, many discrete devices provide an additional terminal labelled SS, resulting in a four-terminal device, such as that appearing in the figure shown above.

- The source and drain terminals are connected through metallic contacts to n-doped regions linked by an n-channel as shown in the figure.The gate is also connected to a metal contact surface but remains insulated from the n-channel by a very thin silicon dioxide (SiO2) layer. SiO2 is a particular type of insulator referred to as a dielectric that sets up opposing electric fields within the dielectric when exposed to an externally applied field. The fact that the SiO2 layer is an insulating layer reveals the following fact:



Depletion Mode Operation

- There is no direct electrical connection between the gate terminal and the channel of a MOSFET.

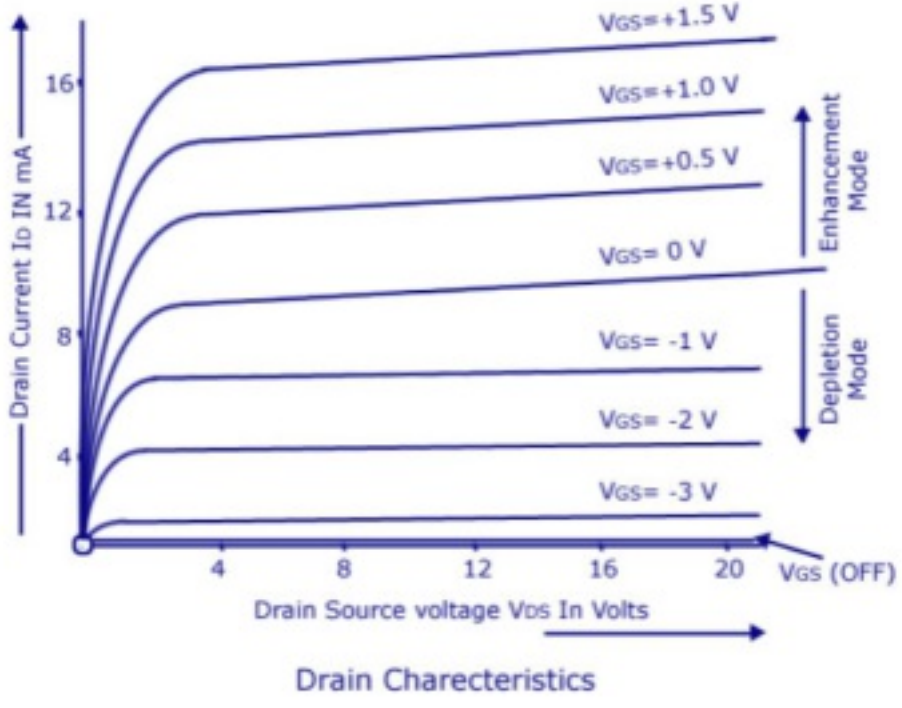
- It is the insulating layer of SiO2 in the MOSFET construction that accounts for the very desirable high input impedance of the device. In fact, the input resistance of a MOSFET is often that of the typical JFET, even though the input impedance of most JFETs is sufficiently high for most applications. The very high input impedance continues to fully support the fact that the gate current (IG) is essentially zero amperes for dc biased configuration

- The reason for the label metal-oxide-semiconductor FET is now fairly obvious: metal for the drain, source, and gate connections to the proper surface in particular, the gate terminal and the control to be offered by the surface area of the contact, the oxide for the silicon dioxide insulating layer, and

the semiconductor for the basic structure on which the n-type and p-type regions are diffused. The insulating layer between the gate and channel has resulted in another name for the device: insulated gate FET or IGFET, although this label is used less and less in current literature.

- In the figure, the gate-to-source voltage is set to zero volts by the direct connection from one terminal to the other and a voltage VDS is applied across the drain to source terminals. The result is an attraction for the positive potential at the drain by the free electrons of the n-channel and a current similar to that established through the channel of the JFET. In fact, the resulting current with VGS = 0 V continues to be labeled IDSS, as shown in the **characteristics of depletion type MOSFET** figure.

- In the figure, VGS has been set at a negative voltage such as 1 V. The negative potential at the gate will tend to pressure electrons toward the p-type substrate (like charges repel) and attract holes from the p-type substrate (opposite charges attract) as shown in the figure.



Drain Charecteristics

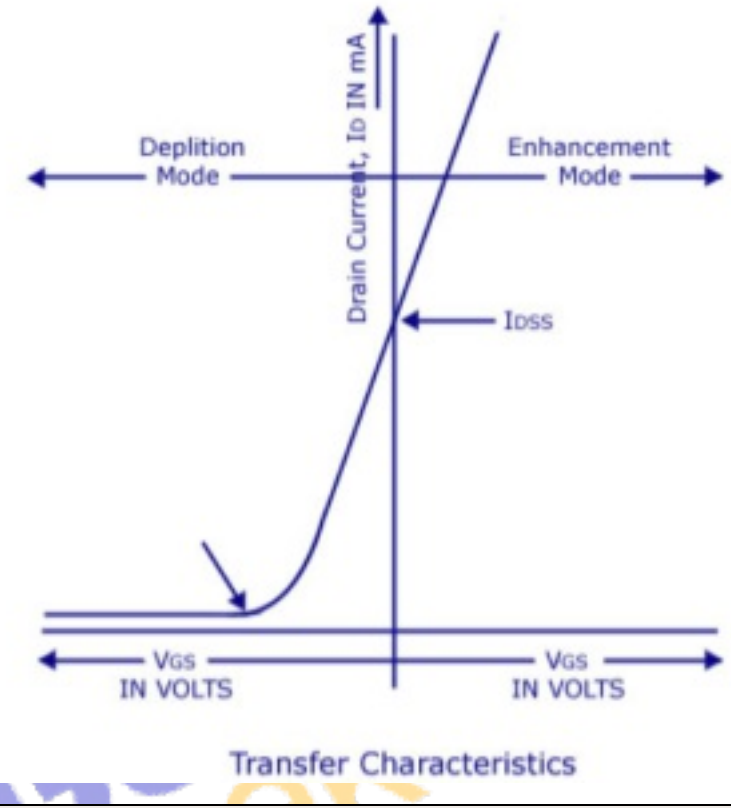
- Depending on the magnitude of the negative bias established by VGS, a level of recombination between electrons and holes will occur that will reduce the number of free electrons in the n-channel available for conduction. The more negative the bias, the higher the rate of recombination. The resulting level of drain current is therefore reduced with increasing negative bias for VGS as shown in the figure below for VGS = - 1 V, - 2 V, and so on, to the pinch-off level of 6 V.

- For positive values of VGS, the positive gate will draw additional electrons (free carriers) from the p-type substrate due to the reverse leakage current and establish new carriers through the collisions resulting between accelerating particles.As the gate to source voltage continues to increase in the positive direction, characteristics of depletion type MOSFET reveals that the drain current will increase at a rapid rate for the reasons listed above.

- The vertical spacing between the VGS = 0 V and VGS = 1 V curves of Fig. 5.25 is a clear indication of how much the current has increased for the 1-V change in VGS.Due to the rapid rise, the user must be aware of the maximum drain current rating since it could be exceeded with a positive gate voltage. That is, for the device of figure showing **characteristics of depletion type MOSFE**T, the application of a voltage VGS = 4 V would result in a drain current of 22.2 mA, which could possibly exceed the maximum rating (current or power) for the device.

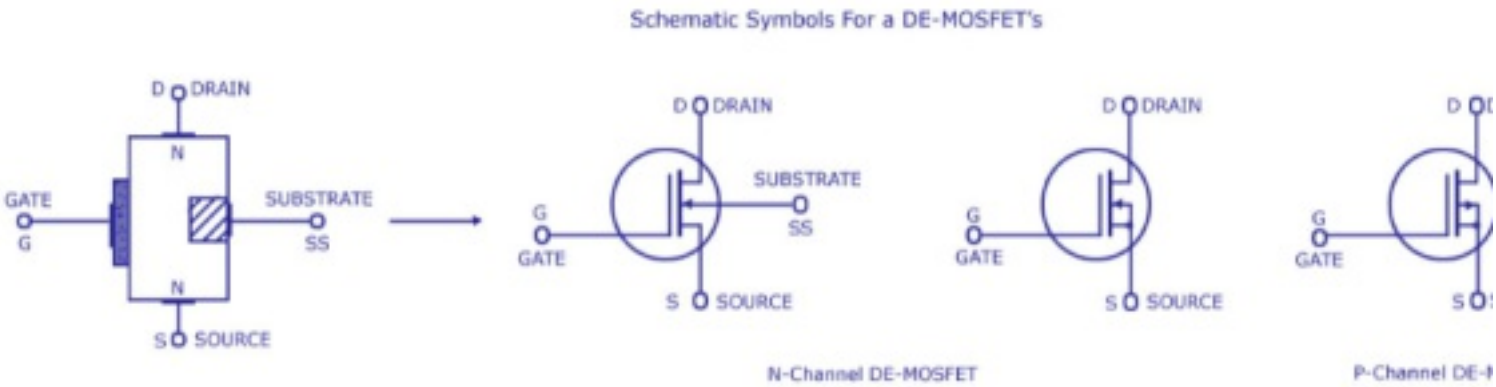
- As revealed above, the application of a positive gate-to-source voltage has “enhanced” the level of free carriers in the channel compared to that encountered with VGS = 0 V.For this reason the region of positive gate voltages on the drain or transfer characteristics is often referred to as the enhancement region,

with the region between cutoff and the saturation level of IDSS referred to as the depletion region.



Transfer Characteristics

- It is particularly interesting and helpful that Shockley's equation will continue to be applicable for the **depletion type MOSFET characteristics** in both the depletion and enhancement regions. For both regions, it is simply necessary that the proper sign be included with VGS in the equation and the sign be carefully monitored in the mathematical operations.



- Figure shows the schematic symbol for a DE-MOSFET. Just to the right of the gate is the thin vertical line representing the channel? The drain lead comes out from the top of the channel and the source lead connects to the bottom. The arrow is on the P-substrate and points to the N-material. In some applications, a voltage can be applied to the substrate for added control of drain current. For this reason, some DE-MOSFETs have four terminal leads. But in most applications, the substrate is connected to the source. Usually the substrate is connected to the source internally by the manufacturer. This results in a three terminal device whose schematic symbol is shown in figure.

- Schematic symbol for a three terminal P-channel DE-MOSFET device is shown in figure. The schematic symbol of a P-channel DE-MOSFET is similar to that of an N-channel DE-MOSFET, except that the arrow points outward.

Question. With labelled diagram explain the construction of n-channel of JFET and also draw its characteristics

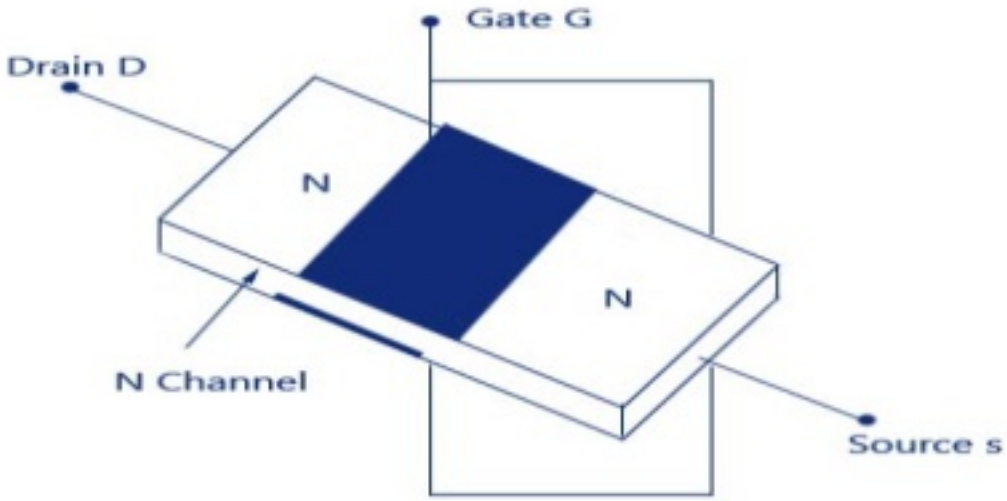
Answer: The structure is quite simple. In an N-channel JFET an N-type silicon bar, referred to as the channel, has two smaller pieces of P-type silicon material diffused on the opposite sides of its middle part, forming P-N junctions, as illustrated in figure. The two P-N junctions forming diodes or gates are connected internally and a common terminal, called the gate terminal, is brought out. Ohmic contacts (direct electrical connections) are made at the two ends of the channel—one lead is called the Source terminal S and the other Drain terminal D.

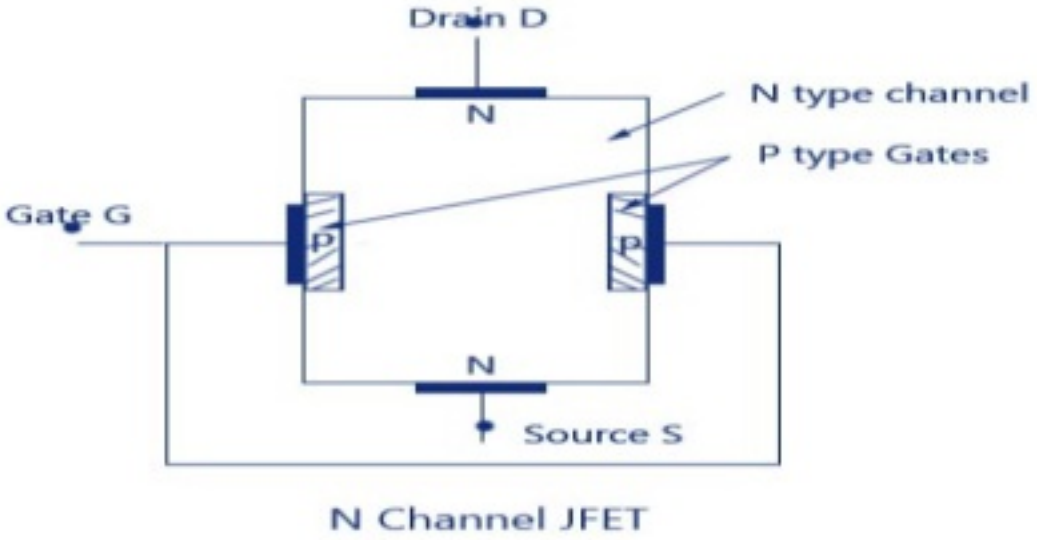
The silicon bar behaves like a resistor between its two terminals D

and S. The gate terminal is analogous to the base of an ordinary transistor (BJT). It is used to control the flow of current from source to drain. Thus, source and drain terminals are analogous to emitter and collector terminals respectively of a BJT.

In the figure above, the gate is P-region, while the source and the drain are N-regions. Because of this, a JFET is similar to two diodes. The gate and the source form one of the diodes, and the drain form the other diode. These two diodes are usually referred as the gate-source diode and the gate-drain diode. Since JFET is a silicon device, it takes only 0.7 volts for forward bias to get significant current in either diode.

With the gate terminal not connected, and a potential applied (+ ve at the drain and – ve at the source), a current called the drain current, ID flows through the channel located between the two P-regions. This current consists of only majority carriers-electrons in this case. P-channel JFET is similar in construction to N-channel JFET except that P-type semiconductor material is sandwiched between two N-type junctions, as shown in figure. In this case majority carriers are holes.





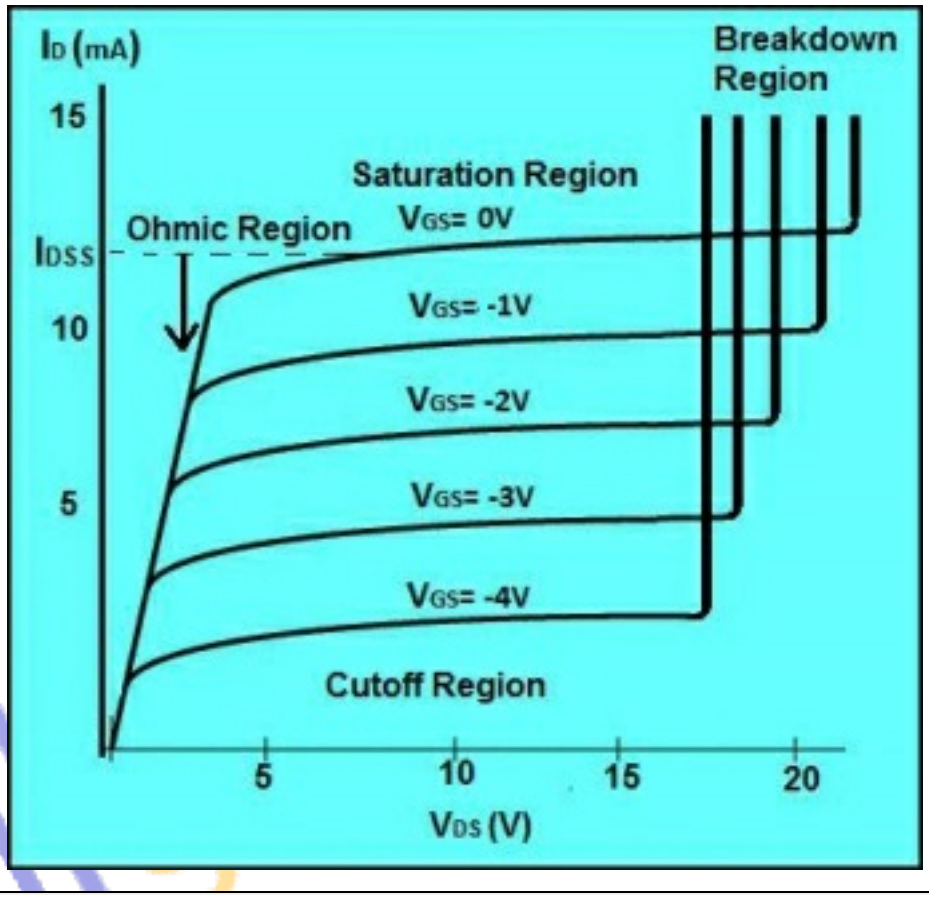
N Channel JFET

The schematic symbols for N-type and P-type JFETs are shown in the figure below. The vertical line in the symbol may be thought as channel and source S and drain D connected to the line.

Note that the direction of the arrow at the gate indicates the direction in which the gate current flows when the gate junction is forward biased. Thus for the N-channel JFET, the arrow at the gate junction points into the device and in P-channel JFET, it is away from the device.

The N-channel JFET characteristics or Trans conductance curve is shown in the figure below which is graphed between drain current

and gate-source voltage. There are multiple regions in the Trans conductance curve and they are ohmic, saturation, cutoff, and breakdown regions.



Ohmic Region

The only region in which trans conductance curve shows linear response and drain current is opposed by the JFET transistor resistance is termed as Ohmic region.

Saturation Region

In the saturation region, the N-channel junction field effect transistor is in ON condition and active, as maximum current flows because of the gate-source voltage applied.

Cutoff Region

In this cutoff region, there will be no drain current flowing and thus,

the N-channel JFET is in OFF condition.

Breakdown Region

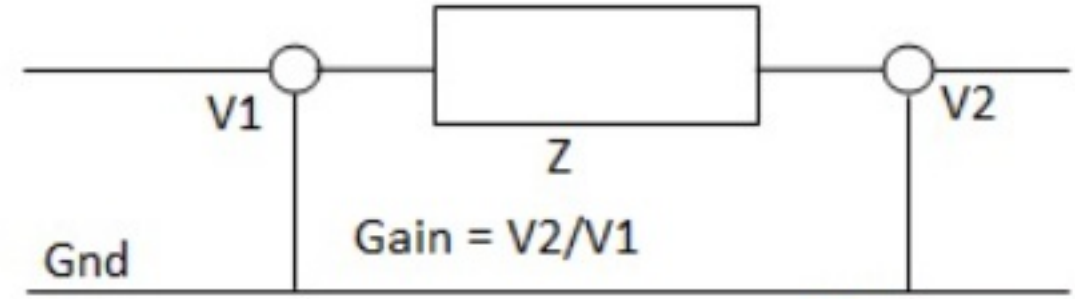
If the VDD voltage applied to the drain terminal exceeds the maximum necessary voltage, then the transistor fails to resist the current and thus, the current flows from drain terminal to source terminal. Hence, the transistor enters into the breakdown region.

Question. Describe Miller effect and derive an equation for Miller input and output capacitor

Answer: The miller effect name is taken from the work of John Milton miller. With the help of Miller theorem, the capacitance of the equivalent circuit of the inverting voltage amplifier can be increased by placing extra impedance between input and output terminals of the circuit. Miller theorem states that a circuit having an impedance (Z), connecting between two nodes where the voltage levels are V1 and V2.

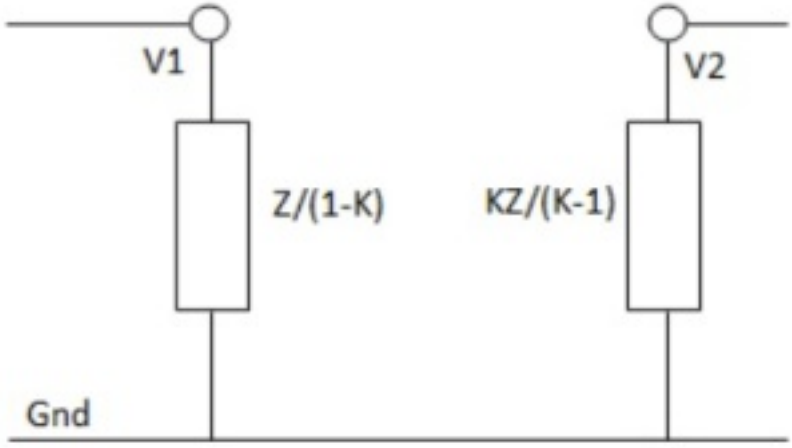
When this impedance is replaced by two different impedance values and connected to the same input & output terminals to the ground for analyzing the frequency response of the amplifier as well as to increase the input capacitance. Such an effect is called a Miller effect. This effect occurs only in inverting amplifiers.

This effect protects the capacitance of the equivalent circuit. At higher frequencies, the circuit gain can be controlled or reduced by the miller capacitance because handling the inverting voltage amplifier at such frequencies is a complex process.



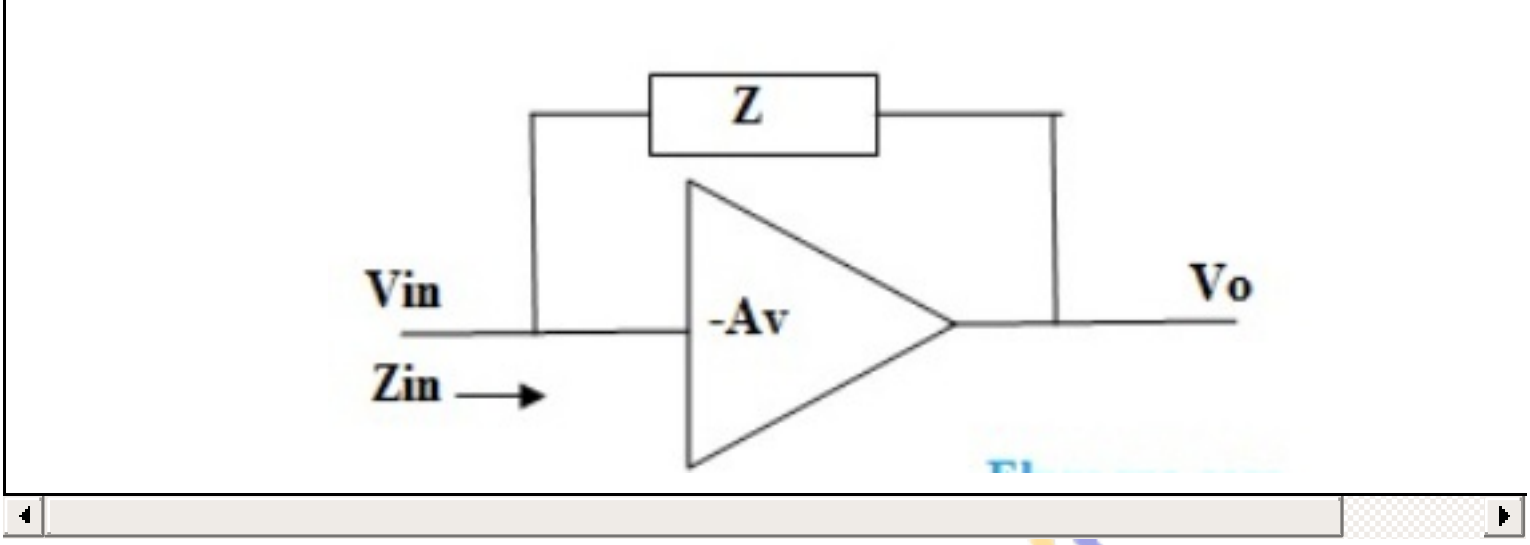
First-miller

If there is some capacitance between the input & output of an inverting voltage amplifier then it will appear to be multiplied by the gain of the amplifier. The additional amount of capacitance will be due to this effect so it is called Miller capacitance.



Second-miller

The below figure shows the ideal inverting voltage amplifier and Vin is the input voltage and Vo is the output voltage, Z is the impedance, the gain is indicated by –Av. And output voltage **Vo = -Av.Vi**



Here, the ideal inverting voltage amplifier attracts zero current and all the current flows through impedance Z.

Then, current **I=Vi-Vo/Z**

I=Vi(1+Av)/Z

The input impedance **Zin=Vi/Ii = Z/1+Av**.

If Z represents the capacitor with impedance, then **Z =1/sC.**

Therefore input impedance **Zin = 1/sCm**

Here **Cm = C (1+Av)**

Cm-miller capacitance.

Question. Briefly explain the characteristics of negative feedback amplifier

Answer: Fundamentally, all electronic devices that provide power gain (e.g., vacuum tubes, bipolar transistors, MOS transistors) are nonlinear. Negative feedback trades gain for higher linearity (reducing distortion) and can provide other benefits. If not designed

correctly, amplifiers with negative feedback can under some circumstances become unstable due to the feedback becoming positive, resulting in unwanted behavior such as oscillation. The Nyquist stability criterion developed by is used to study the stability of feedback amplifiers.

Feedback amplifiers share these properties:

Pros:

- Can increase or decrease input impedance (depending on type of feedback).
- Can increase or decrease output impedance (depending on type of feedback).
- Reduces total distortion if sufficiently applied (increases linearity).
- Increases the bandwidth.
- Desensitizes gain to component variations.
- Can control step response of amplifier.

Cons:

- May lead to instability if not designed carefully.
- Amplifier gain decreases.
- Input and output impedances of a negative-feedback amplifier (*closed-loop amplifier*) become sensitive to the gain of an amplifier without feedback (*open-loop amplifier*)—that exposes these impedances to variations in the open-loop gain, for example, due to parameter variations or nonlinearity of the open-loop gain.
- Changes the composition of the distortion (increasing audibility)

if insufficiently applied.

The most widely preferred amplifier among the two types of the amplifier is the negative feedback amplifier. The characteristics of this amplifier are:

- In the topology of the feedback amplifiers in the voltage series feedback the input impedance value increases and the output impedance decreases.
- In the topology of the voltage shunt feedback, both the input and the output resistances values are decreases.
- In the current series feedback circuits, both the input and the output resistances are increased because of its topology.
- In the current shunt feedback topology, the amplifiers input resistance decreases and the output resistance decreases because of its connectivity of the input, output and feedback circuit.
- In this way, the characteristics are defined based on the various topologies. Each topology defined has its significance of utilization.

Simple amplifiers like the common emitter configuration have primarily low-order distortion, such as the 2nd and 3rd harmonics. In audio systems, these can be minimally audible because musical signals are typically already a harmonic series, and the low-order distortion products are hidden by the masking effect of the human hearing system.

After applying moderate amounts of negative feedback (10–15 dB), the low-order harmonics are reduced, but higher-order harmonics are introduced. Since these are not masked as well, the distortion becomes audibly worse, even though the overall THD may go down. This has led to a persistent myth that negative feedback is detrimental in audio amplifiers, leading audiophile manufacturers to

market their amplifiers as "zero feedback" (even when they use local feedback to linearize each stage).

However, as the amount of negative feedback is increased further, all harmonics are reduced, returning the distortion to inaudibility, and then improving it beyond the original zero-feedback stage (provided the system is strictly stable).So the problem is not negative feedback, but insufficient amounts of it.

Question. Explain positive clipping and negative clamping circuits

Clampers can be broadly classified into two types. They are positive clampers and negative clampers.

1. **Positive Clamper:** This type of clamping circuit shifts the input waveform in a positive direction, as a result the waveform lies above a DC reference voltage.
2. **Negative Clamper:** This type of clamping circuit shifts the input waveform in a negative direction, as a result the waveform lies below a DC reference voltage.

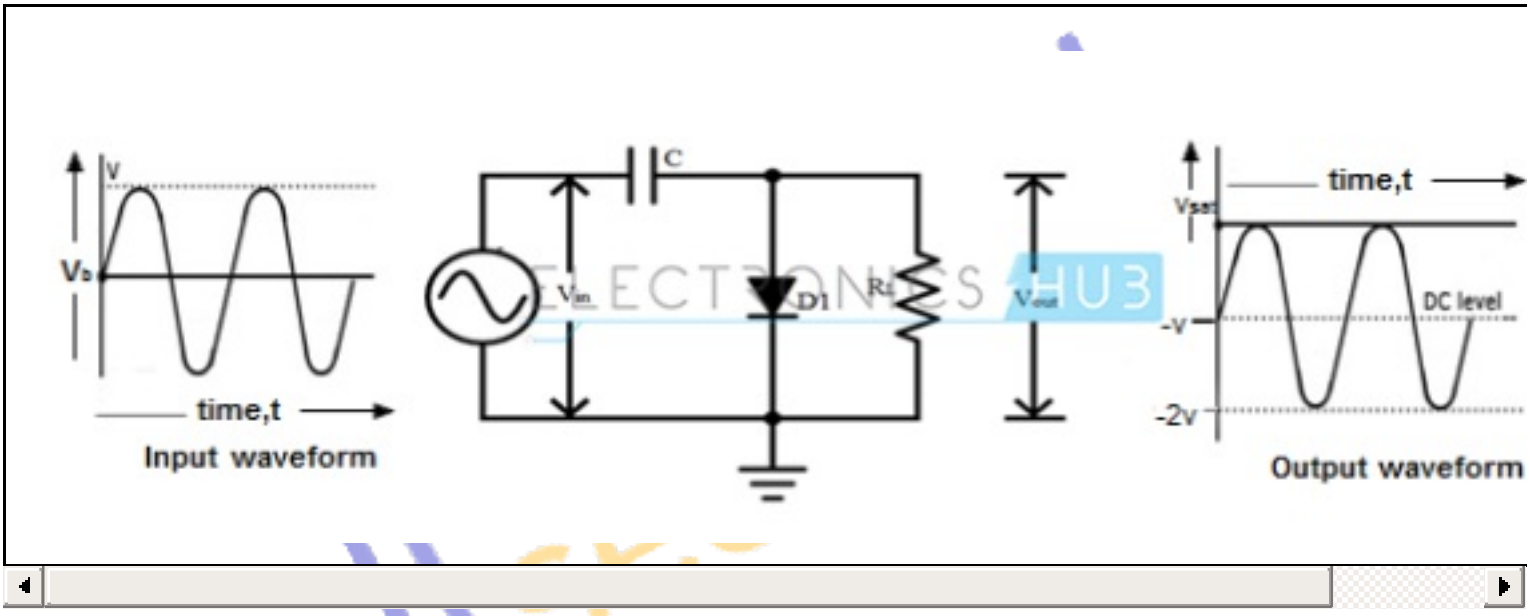
The direction of the diode in the clamping circuit determines the clamper circuit type. The operation of a clamping circuit is mainly based on the switching time constants of the capacitor. However, capacitor in the circuit charges through the diode and discharges through the load.

Negative Clamper

The Negative Clamping circuit consists of a diode connected in parallel with the load. The capacitor used in the clamping circuit can be chosen such that it must charge very quickly and it should not discharge very drastically. The anode of the diode is connected to the capacitor and cathode to the ground. During the positive half cycle of the input, the diode is in forward bias and as the diode conducts the

capacitor charges very quickly.

During the negative half cycle of the input, the diode will be in reverse bias and the diode will not conduct, the output voltage will be equal to the sum of the applied input voltage and the charge stored in the capacitor during reverse bias. The output waveform is same as input waveform, but shifted below 0 volts.



Positive Clamper

The circuit of the positive clamper is similar to the negative clamper but the direction of the diode is inverted in such a way that the cathode of the diode is connected to the capacitor. During the positive half wave cycle, output voltage of the circuit will be the sum of applied input voltage and the charge stored at capacitor. During the negative half wave cycle, the diode starts to conduct and charges the capacitor very quickly to its maximum value. The output waveform of the positive clamper shifts towards the positive direction above the 0 volts.